

12-Bit Rail-to-Rail Micropower DACs in SO-8

January 1995

FEATURES

- 12-Bit Resolution
- **Buffered True Rail-to-Rail Voltage Output**
- 3V Operation (LTC1453), I_{CC} : 250 μ A Typ
- 5V Operation (LTC1451), I_{CC} : 400 μ A Typ
- 3V to 5V Operation (LTC1452), I_{CC} : 225 μ A Typ
- Built-In Reference: 2.048V (LTC1451)
1.220V (LTC1453)
- Multiplying Version (LTC1452)
- Power-On Reset
- **SO-8 Package**
- Three-Wire Cascadable Serial Interface
- **Maximum DNL Error: 0.5LSB**
- Low Cost

APPLICATIONS

- Digital Calibration
- Industrial Process Control
- Automatic Test Equipment
- Cellular Telephones

DESCRIPTION


The LTC[®]1451/LTC1452/LTC1453 are complete single supply, rail-to-rail voltage output 12-bit digital-to-analog converters (DACs) in an SO-8 package. They include an output buffer amplifier and an easy-to-use three-wire cascadable serial interface.

The LTC1451 has an on-board reference of 2.048V and a full-scale output of 4.095V. It operates from a single 4.5V to 5.5V supply.

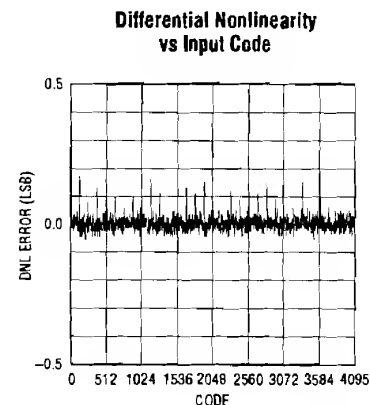
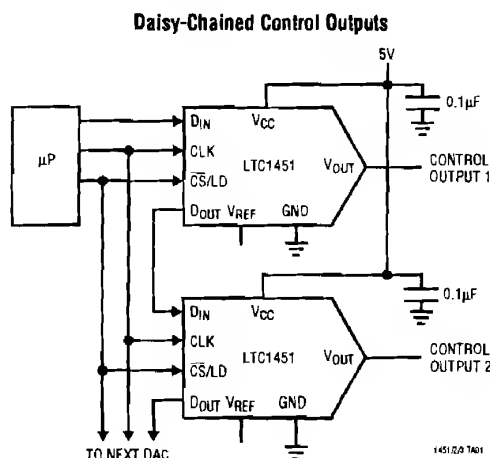
The LTC1452 is a multiplying DAC with a full-scale output of twice the reference input voltage. It operates from a single supply of 2.7V to 5.5V.

The LTC1453 has an on-board 1.22V reference and a full-scale output of 2.5V. It operates from a single supply of 2.7V to 5.5V.

The low power supply current makes the LTC1451 family ideal for battery-powered applications. The space saving 8-pin SO package and operation with no external components provide the smallest 12-bit DAC system available.

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TYPICAL APPLICATION



1451/DQ TA02

LTC1451/LTC1452/LTC1453

ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND	-0.5V to 7.5V	Operating Temperature Range	
TTL Input Voltage	-0.5V to 7.5V	Commercial	0°C to 70°C
V_{OUT}	-0.5V to $V_{CC} + 0.5V$	Industrial	-40°C to 85°C
REF	-0.5V to $V_{CC} + 0.5V$	Storage Temperature Range	-65°C to 150°C
Maximum Junction Temperature	-65°C to 125°C	Lead Temperature (Soldering, 10 sec)	300°C

PACKAGE/ORDER INFORMATION

TOP VIEW		ORDER PART NUMBER		S8 PART MARKING
CLK [1]	[8] V_{CC}	LTC1451CN8	LTC1451CS8	1451C
D_{IN} [2]	[7] V_{OUT}	LTC1452CN8	LTC1452CS8	1451I
CS/LD [3]	[6] REF	LTC1453CN8	LTC1453CS8	1452C
D_{OUT} [4]	[5] GND	LTC1451IN8	LTC1451IS8	1452I
		LTC1452IN8	LTC1452IS8	1453C
		LTC1453IN8	LTC1453IS8	1453I

NB PACKAGE: 8-LEAD PLASTIC DIP
 S8 PACKAGE: 8-LEAD PLASTIC SOIC
 $T_{JMAX} = 125^{\circ}C, \theta_{JA} = 100^{\circ}C/W$ (N)
 $T_{JMAX} = 125^{\circ}C, \theta_{JA} = 150^{\circ}C/W$ (S)

Consult factory for Military grade parts.

ELECTRICAL CHARACTERISTICS

$V_{CC} = 4.5V$ to $5.5V$ (LTC1451), $2.7V$ to $5.5V$ (LTC1452/LTC1453), internal or external reference ($V_{REF} \leq V_{CC}/2$), V_{OUT} and REF unloaded, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC							
	Resolution		●	12			Bits
DNL	Differential Nonlinearity	Guaranteed Monotonic (Note 1)	●			±0.5	LSB
INL	Integral Nonlinearity	T _A = 25°C (Note 1)	●			±3.5 ±4	LSB LSB
V _{OS}	Offset Error	T _A = 25°C	●			±12 ±18	mV mV
V _{OS} TC	Offset Error Temperature Coefficient				±15		µV/°C
V _{FS}	Full-Scale Voltage	When Using Internal Reference, LTC1451, T _A = 25°C	●	4.065	4.095	4.125	V
		LTC1451		4.045	4.095	4.145	V
		External 2.048V Reference, V _{CC} = 5V, LTC1452	●	4.075	4.095	4.115	V
		When Using Internal Reference, LTC1453, T _A = 25°C	●	2.470	2.500	2.530	V
		LTC1453		2.460	2.500	2.540	V
V _{FS} TC	Full-Scale Voltage Temperature Coefficient	When Using Internal Reference, LTC1451			±0.10		LSB/°C
		When Using External 2.048V Reference, LTC1452			±0.02		LSB/°C
		When Using Internal Reference, LTC1453			±0.10		LSB/°C

ELECTRICAL CHARACTERISTICS

$V_{CC} = 4.5V$ to $5.5V$ (LTC1451), $2.7V$ to $5.5V$ (LTC1452/LTC1453), internal or external reference ($V_{REF} \leq V_{CC}/2$), V_{OUT} and REF unloaded, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference (LTC1451/LTC1453)							
	Reference Output Voltage	LTC1451 LTC1453	● ●	2.008 1.195	2.048 1.220	2.088 1.245	V V
	Reference Output Temperature Coefficient				±0.08		LSB/°C
	Reference Line Regulation		●		0.7	±2	LSB/V
	Reference Load Regulation	$0 \leq I_{OUT} \leq 100\mu A$, LTC1451 LTC1453	● ●		0.2 0.6	±1.5 ±3	LSB LSB
	Reference Input Range	$V_{REF} \leq V_{CC} - 1.5V$	●			$V_{CC}/2$	V
	Reference Input Resistance		●	8	14	18	kΩ
	Reference Input Capacitance				15		pF
	Short-Circuit Current	REF Shorted to GND	●			80	mA
Power Supply							
V_{CC}	Positive Supply Voltage	For Specified Performance, LTC1451 LTC1452 LTC1453	● ● ●	4.5 2.7 2.7		5.5 5.5 5.5	V V V
I_{CC}	Supply Current	$4.5V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1451 $2.7V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1452 $2.7V \leq V_{CC} \leq 5.5V$ (Note 4), LTC1453	● ● ●	300 120 150	400 225 250	620 350 500	μA μA μA
Op Amp DC Performance							
	Short-Circuit Current Low	V_{OUT} Shorted to GND	●			100	mA
	Short-Circuit Current High	V_{OUT} Shorted to V_{CC}	●			120	mA
	Output Impedance to GND	Input Code = 0	●		40	120	Ω
AC Performance							
	Voltage Output Slew Rate	(Note 2)	●	0.5	1.0		V/μs
	Voltage Output Settling Time	(Notes 2, 3) to ±0.5LSB			14		μs
	Digital Feedthrough				0.3		nV • s
	AC Feedthrough	REF = 1kHz, 2V _{p-p} , LTC1452			−95		dB
SINAD	Signal-to-Noise + Distortion	REF = 1kHz, 2V _{p-p} , (Code: All 1s) LTC1452			85		dB
Digital I/O							
V_{IH}	Digital Input High Voltage	$V_{CC} = 5V$, LTC1451/LTC1452 $V_{CC} = 3V$, LTC1453	● ●	2.4 2.0			V V
V_{IL}	Digital Input Low Voltage	$V_{CC} = 5V$, LTC1451/LTC1452 $V_{CC} = 3V$, LTC1453	● ●			0.8 0.6	V V
V_{OH}	Digital Output High Voltage	$V_{CC} = 5V$, $I_{OUT} = -1mA$, D _{OUT} Only, LTC1451/LTC1452 $V_{CC} = 3V$, LTC1453	● ●		$V_{CC} - 1.0$ $V_{CC} - 0.7$		V V
V_{OL}	Digital Output Low Voltage	$V_{CC} = 5V$, $I_{OUT} = 1mA$, D _{OUT} Only, LTC1451/LTC1452 $V_{CC} = 3V$, LTC1453	● ●	0.4 0.4			V V
I_{LEAK}	Digital Input Leakage	$V_{CC} = 5V$, $V_{IN} = GND$ to V_{CC}	●			±10	μA
C_{IN}	Digital Input Capacitance	Guaranteed by Design. Not Subject to Test.	●			10	pF

LTC1451/LTC1452/LTC1453

ELECTRICAL CHARACTERISTICS

V_{CC} = 4.5V to 5.5V (LTC1451), 2.7V to 5.5V (LTC1452/LTC1453), internal or external reference (V_{REF} ≤ V_{CC}/2), V_{OUT} and REF unloaded, T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Switching						
t ₁	D _{IN} Valid to CLK Setup	V _{CC} = 5V, LTC1451/LTC1452	●	40		ns
		V _{CC} = 3V, LTC1453	●	60		ns
t ₂	D _{IN} Valid to CLK Hold	V _{CC} = 5V, LTC1451/LTC1452	●	0		ns
		V _{CC} = 3V, LTC1453	●	0		ns
t ₃	CLK High Time	V _{CC} = 5V, LTC1451/LTC1452	●	40		ns
		V _{CC} = 3V, LTC1453	●	60		ns
t ₄	CLK Low Time	V _{CC} = 5V, LTC1451/LTC1452	●	40		ns
		V _{CC} = 3V, LTC1453	●	60		ns
t ₅	CS/LD Pulse Width	V _{CC} = 5V, LTC1451/LTC1452	●	50		ns
		V _{CC} = 3V, LTC1453	●	80		ns
t ₆	LSB CLK to CS/LD	V _{CC} = 5V, LTC1451/LTC1452	●	40		ns
		V _{CC} = 3V, LTC1453	●	60		ns
t ₇	CS/LD Low to CLK	V _{CC} = 5V, LTC1451/LTC1452	●	20		ns
		V _{CC} = 3V, LTC1453	●	30		ns
t ₈	D _{OUT} Output Delay	C _{LOAD} = 15pF, V _{CC} = 5V, LTC1451/LTC1452	●		150	ns
		V _{CC} = 3V, LTC1453	●		220	ns
t ₉	CLK Low to CS/LD Low	V _{CC} = 5V, LTC1451/LTC1452	●	20		ns
		V _{CC} = 3V, LTC1453	●	30		ns

The ● denotes specifications which apply over the full operating temperature range.

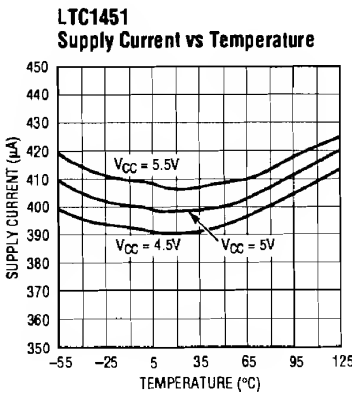
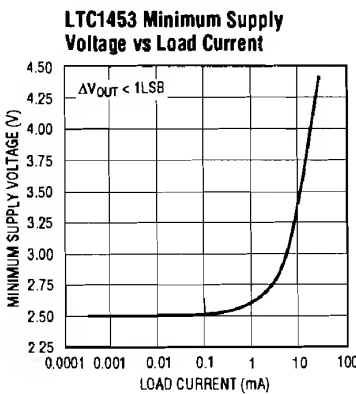
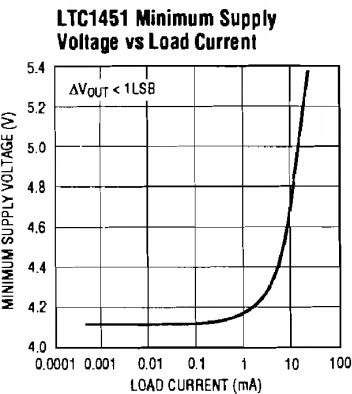
Note 1: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 4095 (full scale).

Note 2: Load is 5kΩ in parallel with 100pF.

Note 3: DAC switched between all 1s and the code corresponding to V_{OS} for the part, i.e., LTC1451: code 18; LTC1453: code 30.

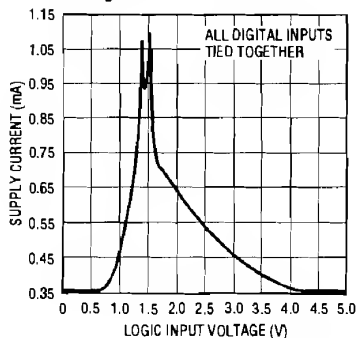
Note 4: Digital inputs at 0V or V_{CC}.

TYPICAL PERFORMANCE CHARACTERISTICS

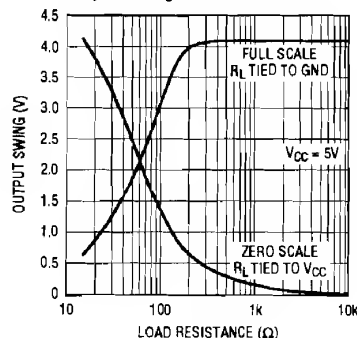


TYPICAL PERFORMANCE CHARACTERISTICS

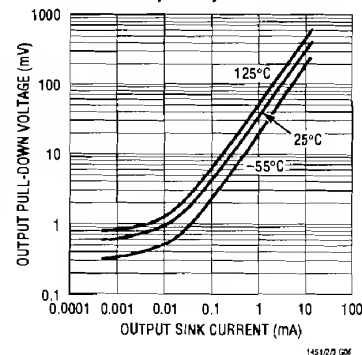
LTC1451
Supply Current vs Logic Input
Voltage



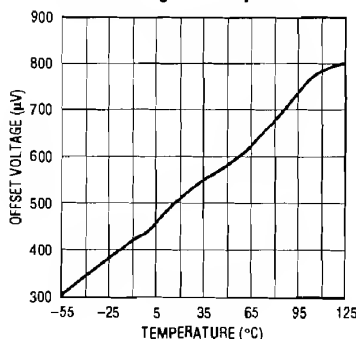
LTC1451
Output Swing vs Load Resistance



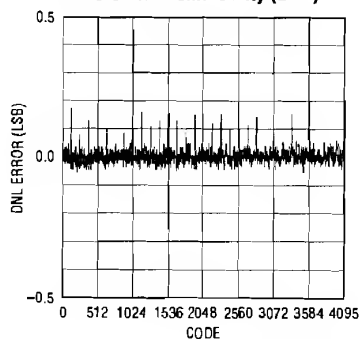
LTC1451
Pull-Down Voltage vs Output Sink
Current Capability



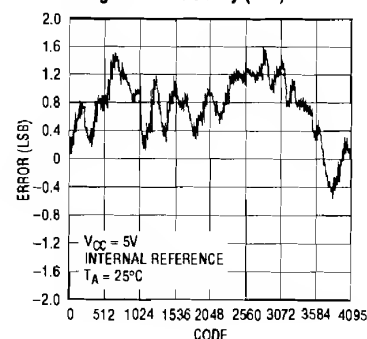
LTC1451
Offset Voltage vs Temperature



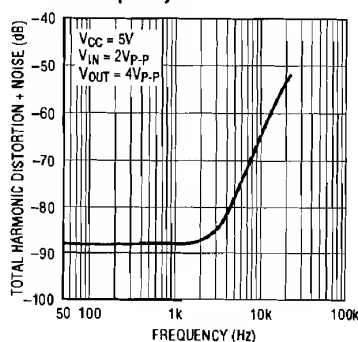
LTC1451
Differential Nonlinearity (DNL)



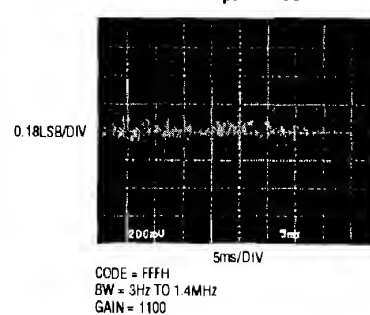
LTC1451
Integral Nonlinearity (INL)



LTC1452
Total Harmonic Distortion + Noise
vs Frequency



LTC1451
Broadband Output Noise



PIN FUNCTIONS

CLK: The TTL Level Input for the Serial Interface Clock.

D_{IN}: The TTL Level Input for the Serial Interface Data. Data on the D_{IN} pin is latched into the shift register on the rising edge of the serial clock.

$\overline{\text{CS/LD}}$: The TTL Level Input for the Serial Interface Enable and Load Control. When $\overline{\text{CS/LD}}$ is low the CLK signal is enabled, so the data can be clocked in. When $\overline{\text{CS/LD}}$ is pulled high, data is loaded from the shift register into the DAC register, updating the DAC output.

D_{OUT}: The Output of the Shift Register which Becomes Valid on the Rising Edge of the Serial Clock.

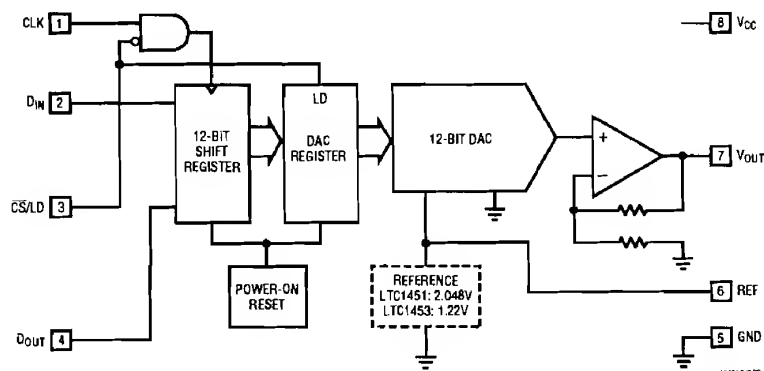
GND: Ground.

REF: The Output of the Internal Reference and the Input to the DAC Resistor Ladder. An external reference with voltage up to $V_{CC}/2$ may be used for the LTC1452.

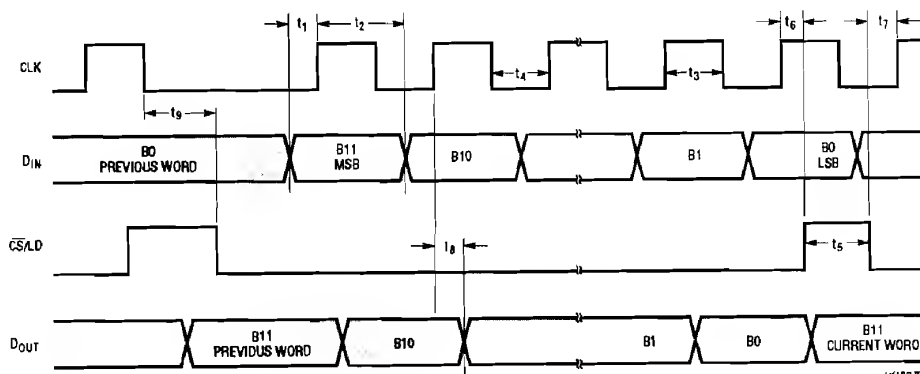
V_{OUT}: The Buffered DAC Output.

V_{CC}: The Positive Supply Input. $4.5V \leq V_{CC} \leq 5.5V$ (LTC1451), $2.7 \leq V_{CC} \leq 5.5V$ (LTC1452/LTC1453). Requires a bypass capacitor to ground.

BLOCK DIAGRAM



TIMING DIAGRAM



DEFINITIONS

Resolution (n): Resolution is defined as the number of digital input bits, n. It defines the number of DAC output states (2^n) that divide the full-scale range. The resolution does not imply linearity.

Full-Scale Voltage (V_{FS}): This is the output of the DAC when all bits are set to 1.

Voltage Offset Error (V_{OS}): The theoretical voltage at the output when the DAC is loaded with all zeros. The output amplifier can have a true negative offset, but because the part is operated from a single supply, the output cannot go below zero. If the offset is negative, the output will remain near 0V resulting in the transfer curve shown in Figure 1.

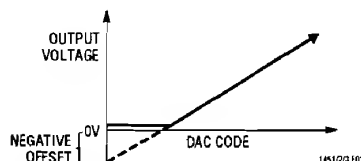


Figure 1. Effect of Negative Offset

The offset of the part is measured at the code that corresponds to the maximum offset specification:

$$V_{OS} = V_{OUT} - [(Code \times V_{FS}) / (2^n - 1)]$$

Least Significant Bit (LSB): One LSB is the ideal voltage difference between two successive codes.

$$LSB = (V_{FS} - V_{OS}) / (2^n - 1) = (V_{FS} - V_{OS}) / 4095$$

Nominal LSBs:

LTC1451	LSB = $4.095V / 4095 = 1mV$
LTC1452	LSB = $V(REF) / 4095$
LTC1453	LSB = $2.5V / 4095 = 0.610mV$

Integral Nonlinearity (INL): End-point INL is the maximum deviation from a straight line passing through the end-points of the DAC transfer curve. Because the part operates from a single supply and the output cannot go below zero, the linearity is measured between full scale and the code corresponding to the maximum offset specification. The INL error at a given input code is calculated as follows:

$$INL = [V_{OUT} - V_{OS} - (V_{FS} - V_{OS})(code/4095)] / LSB$$

V_{OUT} = The output voltage of the DAC measured at the given input code

Differential Nonlinearity (DNL): DNL is the difference between the measured change and the ideal 1LSB change between any two adjacent codes. The DNL error between any two codes is calculated as follows:

$$DNL = (\Delta V_{OUT} - LSB) / LSB$$

ΔV_{OUT} = The measured voltage difference between two adjacent codes

Digital Feedthrough: The glitch that appears at the analog output caused by AC coupling from the digital inputs when they change state. The area of the glitch is specified in nV \times sec.

OPERATION

Serial Interface

The data on the D_{IN} input is loaded into the shift register on the rising edge of the clock. The MSB is loaded first. The DAC register loads the data from the shift register when \overline{CS}/LD is pulled high. The CLK is disabled internally when \overline{CS}/LD is high. Note: CLK must be low before \overline{CS}/LD is pulled low to avoid an extra internal clock pulse.

The buffered output of the 12-bit shift register is available on the D_{OUT} pin which swings from GND to V_{CC} .

Multiple LTC1451/LTC1452/LTC1453s may be daisy-chained together by connecting the D_{OUT} pin to the D_{IN} pin of the next chip, while the CLK and \overline{CS}/LD signals remain common to all chips in the daisy chain. The serial data is clocked to all of the chips, then the \overline{CS}/LD signal is pulled high to update all of them simultaneously.

Reference

The LTC1451 includes an internal 2.048V reference, making 1LSB equal to 1mV (gain of 2). The LTC1453 has an

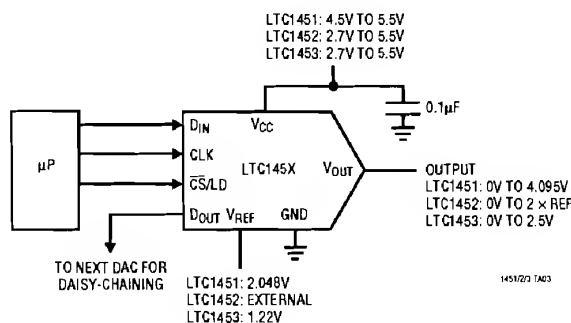
LTC1451/LTC1452/LTC1453

internal reference of 1.22V with a full scale of 2.5V (gain of 2.05). The internal reference output is turned off when the pin is forced above the reference voltage, allowing an external reference to be connected to the reference pin. The LTC1452 has no internal reference and the REF pin must be driven externally. The buffer gain is 2, so the external reference must be less than $V_{CC}/2$ and be capable of driving the 8k minimum DAC resistor ladder.

Voltage Output

The LTC1451 family's rail-to-rail buffered output can source or sink 5mA over the entire operating temperature range while pulling to within 300mV of the positive supply voltage or ground. The output swings to within a few millivolts of either supply rail when unloaded and has an equivalent output resistance of 40 Ω when driving a load to the rails. The output can drive 1000pF without going into oscillation.

TYPICAL APPLICATIONS



An Isolated 4mA to 20mA Process Controller Has 3.3V Minimum Loop Voltage

